

Sujet : Re: EER support?

De : K Jones <kyle.kflorida@gmail.com>

Date : 27/11/2018 à 17:19

Pour : Steve Haynal <softerhardware@gmail.com>

Copie à : hermes-lite@googlegroups.com

Guys.... I wanted to pass the following along that Ruediger sent me yesterday very nice work he is doing:

He Kyle,

Thank you for passing the information. In the meantime have improved my PWM converter with some new features.

The features are:

- Dead time controller
- Over current controller
- Smaler heatsink
- Overcome some further miscellaneous shortcomings

The new PWM version shell drive my new GAN EF2,odd power amplifier stages with Infineon GAN Fets with a 100 volt Envelope supply votage. Also I have developed a centralized digital predriver for the EF2,odd amplifier stages, so I need only one driver for all EF band moduls. I hope Phil and Warren will find time to integrate the predistortion feature for the unmodulated phase signal in EER mode soon.

In the attachments you can find all the new moduls.

Best regards

Ruediger

DJ1MR

On Fri, Nov 23, 2018 at 9:44 AM Steve Haynal <softerhardware@gmail.com> wrote:

Hi Claudio,

Thanks for this work! I saw you pull request. I am still traveling with limited internet. I will be home by next weekend and will do the merge then.

73,

Steve
kf7o

On Wednesday, November 21, 2018 at 2:04:55 PM UTC-8, in3otd wrote:

Hello Steve,

I don't think that a 3.3 V level output for the envelope PWM is mandatory, using a 2.5 V output should be fine since it will be use either to drive a SMPS via a buffer/optocoupler or filtered and amplified to get an analog output. I was looking for a 3.3 V pin just to keep the same levels as in the original Hermes.

In the meantime I've also added the EER controls to linhpsdr, since I usually use Linux for all the ham radio stuff here.

the resemblance to the PowerSDR EER tab is not a coincidence, hi.

The code seems to work fine, below is a screenshot of the RF and the filtered PWM envelope output of a short section of speech when using linhpsdr:

73 de Claudio, IN3OTD / DK1CG

On Monday, November 19, 2018 at 6:44:11 PM UTC+1, Steve Haynal wrote:

Hi Claudio,

There are actually no 3.3V output pins still available. There are several spare input-only due to the FPGA architecture. If you need a 3.3V output pin, some options are:

1. Repurpose one of the LED outputs. They are 3.3V.
2. Use pin 105 from the FPGA. This currently connects to PGA[5] on the AD9866. It is there to

support a future mode of operation but is not currently used. It may be hard to connect to this pin as there are no test pads on the trace.

3. Convert to 3.3V operation for Vlvds. This requires removing FB28 and connecting to 3.3V instead of 2.5V. In early boards there was a footprint for this, but I removed that to simplify things... Then the IO pins are 3.3V. Currently the IO pins are 2.5V to support LVDS communication, which doesn't work with 3.3V bank voltage. LVDS is what I plan to use to link and synchronize multiple HL2s.

73,

Steve
kf7o

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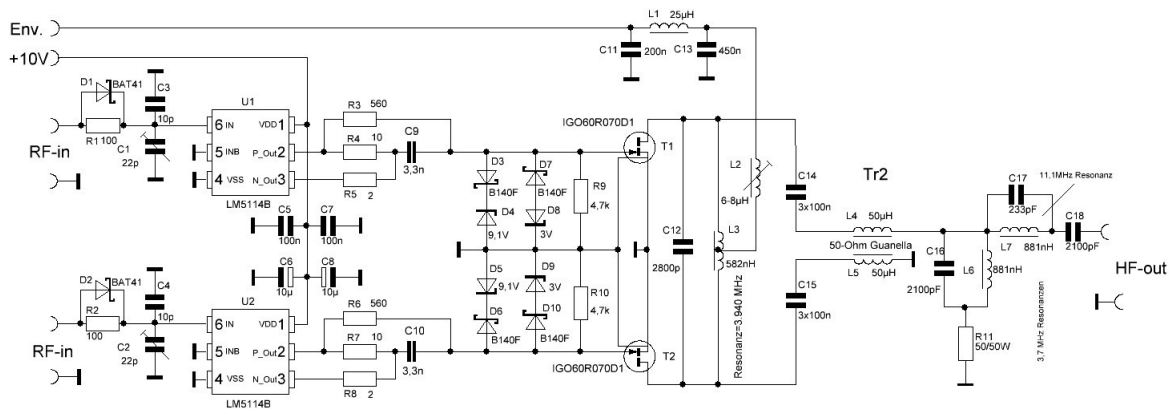
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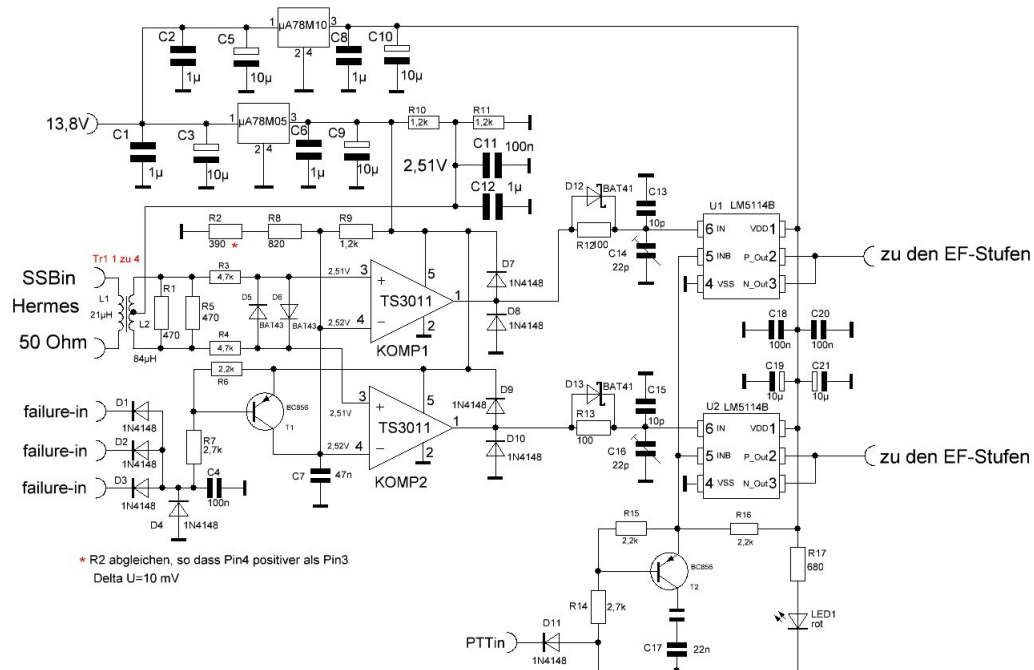
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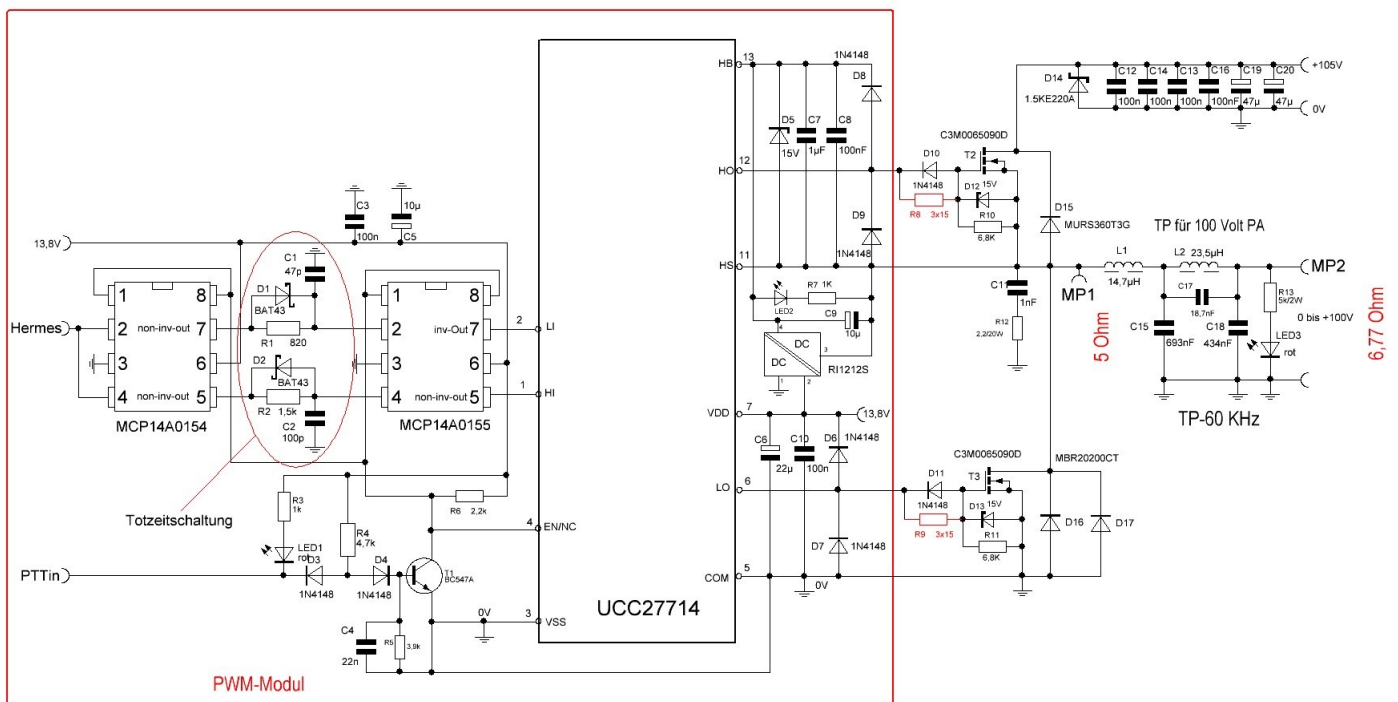


GAN-Fet Hüllkurven PA Endstufe 3,7 MHz/1KW DJ1MR 14.11.2018

— Digital-Treiber.jpg —



Digital-Treiber EF-Endstufen DJ1MR 17.11.2018



Schaltplan-26.11.2018 mit Totzeitschaltung

—Pièces jointes :—

PWM-Basic-PCB.JPG	1,7 Mo
EF-Endstufe-digital-GAN-Fets.jpg	148 Ko
Digital-Treiber.jpg	186 Ko
Controller-PWM-Current.jpg	877 Ko
Erster Test EF Digitaltreiber DJ1MR.PDF	1,2 Mo
Current-Controllert.jpg	131 Ko
PWM-circuit-diagramTotzeit.jpg	217 Ko